SEEKER ELECTRONICS

Tiger Sharc DSP Processor (TS201S)	600 MHz- Two Processors
Boot Flash	512 KB
Application Flash	512 KB
SRAM	512 KB
DACs	2
DDC Chips	3
RS422 Channels	4
TTL-DIPS	4
TTL-DOPS	4
External Clock Provision	Yes
Xilinx-FPGA	XC5VLX50-2FFG1153I
PROM	XCF32PV048C
Programming	Through JTAG Header
Saw Filter Specifications	
Input	70MHZ
Bandwidth	4MHZ
Input Impedance	50ohms
Pass band ripple	0.5dB
Stop band attenuation(>=73MHZ)	55dB
Input Clock	
Input	80 MHz, Sine wave
Signal level	0dBm
Input Impedance	50 ohms
Input Connector	SMA
Digital Down Conversion Specifications	
Number of Input Channels	3
Number of parallel digital ltering	3
Integrated ADC	14 bit, 80 MSPS
IF Sampling Frequencies	Up to 200 MHz
Output Sampling frequencies:	Programmable up to 80 MHz
Output Data from DDC	16 bit, I & Q data on all the channels
Analog Input Specifications	
No of Channels	3
IF frequency	70MHZ
Bandwidth	±2MHZ,max
Signal level	-100dBm,min. 0dBm,max
Input Impedance	50 ohms
Input polarity	Bipolar, single ended
Dynamic Range	-120dBm
Sampling Frequency	80 M Hz
Input Connector	SMA

* Note : Specifications are subject to change without notice