Tiger Sharc DSP-Signal Processor

DESCRIPTION

Tiger Sharc DSP-Signal Processor is a combination of higher end Virtex-II Pro Xilinx FPGA and Tiger Sharc DSP. A DSP running at 600MHz along with a softcore Power PC built in FPGA makes the system ideal for higher end processing requirement. The system also has two ADC Channels and multiple General purpose I/Os. All necessary support files and sample code along withapplication development support can be provided.

SPECIFICATIONS

- ADSP-TS201SABP @ 600MHz
- Xilinx Virtex II Pro-XC2VP40 FPGA
- SRAM Memory: 512K x 32K Bits
- 14 bit ADC : 2 ch
- Input range : -1V to +1V
- Frequency : min=50KHz, max=2MHz
- ADC Fs: 2MHz to 40MHz
- ADC Range : 0-2V
- ADC sample clock : EXT/INT
- No of Interrupts 1,Differential, TTL Buffered
- Sampling clocks : 2
- Provision to configure either internal or external, TTL
- No of Flags 4, Software configurable as I/P or O/P
- 8 Digital Inputs, TTL Buffered
- Propagation delay : ~5nsec (Max)
- Input Supply Voltage : 28V ±4V
- 16 Outputs, TTL Buffered
- Buffered Specification : Current : 24mA
- Propagation Delay : ~5nsec (Max)
- Voltage : 5V tolerable
- Clock Output 1
- Frequency : 2MHz to 40MHz
- Steps : 40MHZ,20 MHz,10 Mhz,5 Mhz,2.5 MHz
- Watch Dog Timer Output 1,TTL, buffered
- Telemetry Signals System Computer Interface 28 V ±4 V Power Supply monitor
- Programmable RS232/RS422 Asynchronous Serial Port @115.2Kbps or high
- TX/RX Interface +10 V, 2A
- Dimensions 240mm x 190mm x 25mm
- Operation Temperature: -40ºC to +85ºC

* Note : Specifications are subject to change without notice