HIGH SPEED SATLLITE DATA RECORDER AND REPLAY SYSTEM (HSDR)

Specification:

Apollo introducing fastest Quad channel Satellite Data Recorder and Replay System. This is Based on high - performance high - reliability PCI-X based server architecture with dual / quad Xeon processors. Mirrored system drives hot swap fans & redundant power suppiles. it provides a 10/100 Ethernet interface for high speed network data transfer. The product offered is well proven & standardized in various satellite programmes of ISRO.

The system accepts serial data & clock up to four Data Streams each channel upto 320Mbps data rate and performs frame synchroniization, derandomization serial to parallel conversion, time and status tagging,... and real time data logging to disk. it can also supports Convolution Decoding and CCSDS RS decoding.

it can also generate a synchronous serial data stream to playback previous recorded data, or to generate a simulated data stream.

KEY FEATURES

- *4 Serial each can support up to 320Mbps*
- *8 Parallel channels each can support upto 20 Mbps*
- *Channel width Configurable as 8, -6 or 32 bit*
- *Each serial channel have independent Data, clock & sync signal*
- *Adjustable delay logic between clock and data channels for proper data latching*
- *Real Time Display for Frames elapsed (X10K),Frame Loss*
- *LED indications for search, check, lock, derandamization, Acquisition status*
- *Real-time disk logging configurable in Raid 0/3/5.*
- *High-speed network transfer*
- *user-friendly Graphic user interface (GUI)*
- *Customization as per specific uder requirement*

INPUT SPECIFICATIONS

Data Rate per Channel : 100 bps to 320Mhps .
No of Channel : Four
Input Signal Type : LVDS standard
Signals : Data with associated Clock
Adjustable Delay : Adjust clock phase using the nternal delay logic (The data delay will be in steps from 0 to15, with each step being 250 ps) so as to ensure proper latching of the signal at the front end.
Data Polarity : Normal and Invert programmabae
Clock selection : As per table

	Clock - 1	Clock - 2
Data - 1	✓	✗
Data - 2	✓	✗

	Clock - 3	Clock - 4
Data - 3	✓	✗
Data - 4	✓	✗

Time code interface : IRIG-A /B/G standard Modulated Time Code signal on a BNC connector.

FRAME SYNCHRONIZER

Frame Sync Code (FSC)

Length : Selectable either 64 or 128 bits
Code : Programmable.
Frame length : Up to maximum of 4Mhits I frame, user programmable

Sync bit Error threshold : 0 to 14 bits programmable.
Bit slip window : 1 to +/-14 bits programmable.
Flame sync Strategy : Search, Check, Lock strategy, Search and Check fixed to one.
Miss in Look : 1 to 14 frames programmable.

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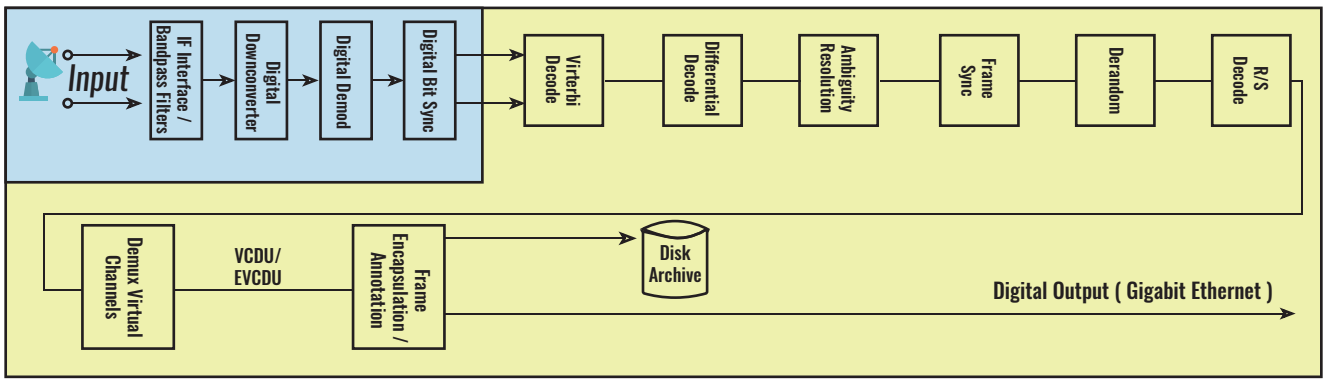

De-RANDOMIZATION

Enable 1 Disable provision

Seed Word	:	*Programmable.*
Length	:	*11 to 16 bits programmable*
Start 01 De-Randomization	:	*64 to 144 bits programmable*
Feedback selection	:	*Feedback is the Ex-OR of two bits. Each of these bits can be selected from any of the 1st-MSB bit of register, whose length is equal to the length of the seed word.*

LBT STRIPPING

Provision to strip out the Low Bit Rate Telemetry (LBT) coming in the High bit Raie Stream and transfer through RS232Ethernet interface. Stripping mechanism is to look for the change in LBT address and pick up the LBT data only once at every change in address. Provision to strip more data slots for a single address slot is available. Frame drop & frame elapsed measurement : Summary logging of the from panel display

DIFFERENTIAL DECODING

Enable/disable Option (Algorithm provided by the user)

SERIAL DATA ACQUISITION

Channel Type	:	*All or Selected Data Collection. In case of selected channels, channel numbers to be specified Capability to handle varying number of bits/S-word :*
Formatted data transfer	:	*Aframe of data consists of a number of Swords and the number of 'bits/S-word' may vary for different satellitesIt. Is possible to acquire such data and assemble them into S-words by programming the number of 'bits/S-word'. Programmability is exist for defining from 6 to 16 bits/S-word separately for each channel. Real time alignment will be done and aligned S-word length will be 8 bits in case of no. of bits/S-word < 8 and 16 bits in case it is >8 and <16 and LSB justified.*
Unformatted data transfer	:	*The incoming serial data will be converted to 32 bit parallel data from the beginning of the frame aligned with FSC and transfer to Disc.*

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SERIAL DATA ACQUISITION START MODES

Normal Mode : *In this mode when ever data acquisitiun is initiated. the data acquisition starts from ihe beginning of the immediate occurrence of the FSC.*

Conditional Mode : *Pattern Detect Siari: In this mode any consecutive S-words (maximum 6, minimum 1) in a frame shall be de-commutaied and compared with a pre-programmed value. The data acquisition shall begin from the beginning ofihe frame in which The comparison is successful. Programmability exists to feed Number of S-words, no. of bits. S-word numbers, number of bits , Valid bit numbers from each S-word and decimal / hex value to be matched.*

Time Code (TMCD) Start Mode : *in this mode the start of acquisition is initiated when the time read from the time code interface matches or just crosses the programmed time. In a similar way data acquisition termination also can be programmed.*

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DATA PLAYBACK / DATA SIMULATOR

No. of channets : *Two (E1, 01) Each channel shall have Data, Clock*

Signal level : *LVDS.*

Data rate : *00 bps lo 320 Mbps / channel when internal clock is selected. data rate is programmable from 100 Mbps to 320 Mbps such that the data rate will be within 0.2% of the desired data rate.*

Cluck selection : *Internal/External for each channel independently is possible to select I1 clock for Q1 channel and I2 clock for Q2 channel. is possible to select I1 clock for all the channels and SMA connector is used for external clock interface.*

Data Simulator : *Configurable simulation and file playback capability for loopback testing (two channel playback loop back to two channel cquisition)*

S-Word Length : *6 to 16 bits/S-word independently for each channel*

Frame Length : *128 bit to 4 M bits maximum*

Dam Pattern : *Programmable*

AA55

Incremental / decremental pattern

Channel ID programmable

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STANDALONE DATA SIMULATOR

All Features are same as Data Playback/Data Simulator except Onboard 2 GB memory for high speed simulation with user image data.

TIMECODE READER SPECIFICATION

IRIG Code types IRIG A, B, G

REED-SOLOMON DECODING

No of bits/symbol	:	*8 bits*
No of symbols per codeword	:	*255*
No of information symbols par code word	:	*223*
No of check symbols per codeword	:	*32*
Decoder Detection and Correcfion Errors	:	*16*
Symbol Formals	:	*Serial & Parallel*

OPTIONAL FEATURES

CONVOLUTIONAL DECODING

CCSDS rate 1/2,constraint length=7

Symbol Formats: Serial 8. Parallel

LED INDICATIONS

Search, check, lock, derandamization enable, Acquisition mode

REAL TIME DISPLAY

Frames elapsed (X10K)

Frames Loss

Current Line Count

APPLICATIONS

- *Reception and processing of high data rate signals from aircraft, LEO or GEO satellites.*
- *Turnkey reception and demodulation for high data rate scientific, remote sensing and telecommunications applications*
- *High-Bit rate remote sensing ground stations*
- *Satellite / Payload Integration and test*
- *High-rate digital Data record/playback system*
- *Satellite link emulation, testing and monitoring*
- *Aircraft data acquisition*
- *High-precision doppler measurement*
- *High-reliability ground station radio*
- *High data rate full duplex radio*

PARALLEL DATA ACQUISITION

Data Rate per Channel	:	*Up to 20 MBps*
No. of Channels	:	*Eight*
Mode	:	*Each Channel can be configured as a input or output.*
Signal type	:	*TTL standard*
Signals	:	*Data with associated clock ans sync signal*
Adjustable delay	:	*Adjust clock phase using the internal delay logic (The data detay will be in steps from 0 to 15, with each step up to 4 ns) so as to ensure proper latching of the signal at the front end.*