DSSS DE-MODULATOR 50Mchips/s

SPECIFICATIONS

Input frequency	70 MHz±25Mhz
No of Frequency Channels	4
Input Sensitivity	- 40dBm
Dynamic Range	0 to -40dBm
Signal bandwidth	≈ 25 MHz
De-Modulation	BPSK/QPSK
Doppler range	± 20 KHz
Spreading code	Programmable(Gold Codes, Marker, Max Length Sequence etc)
Cold start Acq time	< 30 msec
Warm start Acq time	< 4 msec
Communication channels	RS 485 -1 No and RS 422- 2 Nos, Gigabit Ethernet-1 No, USB 2.0 HDLC Asynchronous - Synchronous Interface
Symbol Data rate	38.5Kbps to 14.2 Mbps
Long term bit rate	TBD
Others	It perform spread sequence acquisition and tracking by correlation or matched filtering
Error Correction Decoding	**Viterbi :** It performs Decoding of convolution code with all four channels simultaneously. IP Cores for these functions to be provided along with supplies
Decimation	Variable (4,8,16,32)
Ancillary Functions	BER measurement PRBS-11 test sequence generator AWGN IP Cores for these functions to be provided along with supplies
Maximum chip rate	**50 Mchips/s**
DSSS spreading factor	**7 to 2047, Gold codes**
FPGA	Xilinx Spartan-6 FG(G)676 package, compatible with LX75,LX100 and LX150. The FPGA is expected to run with a processing clock in the range 100 to 120 MHz
ADC	Four Channel 14-bit ADCs, 210Mbps
DDR2 Memory for FPGA	N/a
Ethernet	Two Gigabit Ethernets to be provided
USB Interface	USB 2.0 Interface to be provided for FPGA
FPGA JTAG connector	Yes
Microcontroller Specifications	⊗ ARM Cortex-M3 NXP1759 for FPGA configuration Microcontroller ⊗ USB Interface ⊗ 2Gb Nand Flash Memory to store FPGA configurations
Typical FPGA configuration time	< 5s Supply voltage : +5V DC +/- 5%
PCB Dimensions	Size : 12cm x 12cm
Temperature Range	-40 to +85 Deg
Parameters Programmability	Through USB/ ETH/RS 232 from GUI

* Note : Specifications are subject to change without notice