

PCI-X BASED 2 CHANNEL SERIAL DATA ACQUISITION CARD



Specification:

PARAMETER	DESCRIPTION
Number of channels	Two (up to 4 Channels).
Input Data Rate	200 Mbps per Channel.
Input Signal Level	LVDS.
Inputs	00 Clock and Data.
Clock polarity	Normal or Invert
Data polarity	Normal or Invert
Clock to Data delay	Max of 4 ns in steps of 250 ps.
Bits per Frame	6 to 16.
Words per Frame	256K (Max).
FS Code Length	128 Bits.
Reference FSC Length	Programmable 128 Bits.
Mask Pattern Length	Programmable 128 Bits.
Frame Sync Code (FSC)	<ul style="list-style-type: none"> ◆ Length: up to 128 bits programmable ◆ Code: Programmable.
Lock Loss Status	Programmable 1 to 14.
Bit Slip	Programmable ± 7 Bits
Error Threshold	Programmable 0 to 15 Bits.
Frame length:	Up to maximum of 16Mbits/frame, programmable
Error allowance:	0 to 14 bits programmable.
Bit slip window:	1 to ± 14 bits programmable.

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Frame sync Strategy:	<i>Search, Check, Lock strategy, Search and Check fixed to one.</i>
Miss in Lock:	<i>1 to 14 frames programmable.</i>
Differential Decoding:	<i>Enable/disable.</i>
<p>De-Randomization: Enable / Disable provision.</p> <ul style="list-style-type: none"> ◇ Seed Word : Programmable. ◇ Length : 11 to 16 bits programmable ◇ Start of De-randomization : 64 to 144 bits programmable ◇ Feedback selection : Feedback is the Ex-OR of two bits. Each of these bits can be selected from any of the 1st – MSB bit of the shift register, whose length is equal to the length of the seed word. 	
<p>LBT Stripping :</p> <p><i>Provision is existed to strip out the Low Bit Rate Telemetry (LBT) coming in the High bit Rate Stream and give user as per RS232C interface through a 9-pin D-type connector. Baud rate 115K, No parity, one stop bit. Stripping mechanism is to look for the change in LBT address and pick up the LBT data only once at every change in address. Provision to strip more data slots for a single address slot is also available. Finally all channels LBT is available on Ethernet the following are the list of configuration parameters for LBT.</i></p> <ul style="list-style-type: none"> ◇ LBT mode ◇ Periodicity Cnt Width ◇ Start bit extract ◇ No of data bit extract ◇ LBT Blk width ◇ LBT Add chg bit ext ◇ Start pos of LBT Blk 	
Bits per Word	<i>6 to 16.</i>
Words per Frame	<i>256K (Max).</i>
Acquisition Modes	<i>Two.</i>
A. Normal	<p><i>Data is acquired from the beginning of the Frame with reference to the Tally Pulse immediately after the acquisition has been initiated one of the modes</i></p> <ul style="list-style-type: none"> <i>a) good frames only</i> <i>b) good frames+ Bad frames</i>

<i>B. Conditional</i>	<i>The incoming the data is checked for the user specified 32-Bit reference code at the user specified position taking into account used the user defined 32-bit mask pattern</i>
<i>Data Transfer Modes</i>	<i>Two.</i>
<i>A. Full Line Transfer</i>	<i>The entire frame of data is transferred</i>
<i>B. Windowed Transfer</i>	<i>Only part of the frame is transferred ,from the user specified S-word and the transfer is for the user defined number of S-words Through Ethernet/RS232</i>
<i>LBT Extraction</i>	<i>Over seven segment Displays/Over GUI screen</i>
<i>Frames elapsed, Frames lost, FSC & status LEDs</i>	<i>Configuration</i>
<i>Real Time merging of Two channels</i>	<i>Upto System RAM / DISC logging using external RAID Unit with</i>
<i>Data logging</i>	<i>MAX 200Mbps/channel. The volume of data acquired to disc during real time for selected channels should be limited to Disc capacity of the raid unit.</i>
TIME CODE READER & GENERATOR <i>Formats : IRIG –A / IRIG –B</i> <i>Signal type : Modulated AM</i> <i>Mark to space Ratio : 3 :1</i> <i>Signal Level : MAX 10 Vpp</i> <i>Connector Type : BNC</i>	Data rate <i>100 bps to 200 Mbps / channel when internal clock is selected, data rate is programmable from 100 bps to 200 Mbps such that the data rate will be within 0.2% of the desired data rate.</i> Clock selection <i>Internal / External for each channel independently selection is possible to select I1 clock for Q1 channel and I2 clock for Q2 channel and also possible to select I1 clock for all the channels and SMA connector is chosen for external clock interface.</i>

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PLAYBACK MODE

Playback file : Real time satellite data acquired file/user specified file

Configuration : Similar to acquisition parameter

Data Rate : up to 200Mbps per channel , channel wise independent

Clock source : Onboard clock (210 MHz) in steps of binary/ external.

No. of channels : 4 Channel

Signal level : LVDS level

S-word length : 6 to 16 bits/S-word independently for each channel

Frame length : 128 bit to 16 M bits maximum

Data pattern

Data pattern: Programmable

Video:

- ◆ Constant Pattern
- ◆ Incremental / decremental pattern
- ◆ Image 64MB per channel.

Aux:

- ◆ Line to line varying pattern etc to be simulated.
- ◆ Channel ID

PRBS 27 -1:

- ◆ Bits per S-word -8
- S-word per Frame -2032

OS Support

WindowsNT/2000, Linux.

Input Connectors

LVDS : 25 Pin D- sub Male.
ECL-SE : SMA Connectors